

Asynchronous arbiter for micro-threaded chip multiprocessors

This paper presents a scalable and partitionable asynchronous bus arbiter for use with chip multiprocessors and its corresponding pre-layout simulation results using VHDL. The arbiter exploits the advantage of a concurrency control instruction (Brk) provided by the micro-threaded microprocessor model to set the priority processor and move the circulated arbitration token to the most likely processor to issue the create instruction. This mechanism provides latency hiding during token circulation by decoupling the micro-threaded processor from the ring's timing. The arbiter provides a very simple arbitration mechanism and can be used for chip multiprocessor arbitration purposes.